LOW POWER FLIP-FLOP DESIGNS FEATURING EFFICIENT EMBEDDED LOGIC

Shefalie Vincent, Bisni.O, Lubna Kareem

Abstract--A DML mode logic is introduced here which improves the speed performance of the design, also achieving significant energy consumption reduction. The large capacitance in precharge node is eliminated by the DDFF and DDFF-ELM designs by following a split dynamic node structure. The DDFF offers power reduction. The DDFF-ELM reduces pipeline overhead. 4-b Johnson up-down counter is used to magnify the performance improvement of the designs, to which the DML logic is introduced. An area, power, and speed efficient method is presented here that incorporates complex logic functions into the flip-flop. The DML logic used in DDFF-ELM helps to achieve low power and high speed requirements.

Index terms-- DML Logic, embedded logic, flip flops, high speed, low power, critical path, counter.

1 INTRODUCTION

Technology and speed are always moving forward, from low scale integration to large and VLSI and from megahertz (MHz) to gigahertz (GHz). The system requirements are also rising up with these continuous advancing processes of technology and speed of operation. In synchronous systems, high speed is being achieved using advanced pipelining techniques. In modern deep pipelined architectures, pushing the speed further up demands a lower pipeline overhead. This overhead is the latency associated with the pipeline elements, such as the flip-flops and latches. Extensive work has been devoted to improve the performance of the flip-flops in the past few decades [2],[3], [6],[7], [8].

A recent paper [4] introduced a flip-flop architecture named cross charge control flip flop (XCFF), which has considerable advantages over SDFF and HLFF in both power and speed. It uses a split-dynamic node to reduce the precharge capacitance, which is one of the most important reasons for the large power consumption in most of the conventional designs. But this structure still has some drawbacks, due to redundant power dissipation that results when the data does not switch for more than one clock (CLK) cycles.

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A new dual dynamic node hybrid flip-flop (DDFF) and a novel embedded logic module (DDFFELM). Both of them eliminate the drawbacks of XCFF. The new designs are free from unwanted transitions resulting when the data input is stable at zero. DDFF-ELM presents a speed, area, and power efficient method to reduce the pipeline overhead. It can be analyzed that the DDFF and DDFF-ELM designs are well suited for modern high-performance designs where power dissipation and latching overhead are of major concern.

The DML logic gates family was proposed in order to provide a very high level of energy-delay (E-D) optimization flexibility [10], [11]. DML allows an on-the-fly change between two operational modes at the gate level: static mode and dynamic mode. In the static mode, DML gates consume very low energy, with some performance degradation, as compared to standard CMOS gates. Alternatively, dynamic DML gates operation obtains very high performance at the expense of increased energy dissipation. A DML basic gate is based on a static logic family gate, e.g., a conventional CMOS gate, and an additional transistor. While DML gates have very simple and intuitive structure, they require an unconventional sizing scheme to achieve the desired behavior [10], [11].

To meet the delay requirements of CPs along with lowering the over-all energy consumption of the design, the powerful modularity of DML is utilized. We propose and analyze a new approach, which locates the design's CPs and utilizes the on-the-fly modularity of DML to operate these paths in the boosted (dynamic) performance mode. The non-critical paths are operated in the low energy static DML mode, which does not affect the performance of the design. The non-critical paths are operated in the low

energy static DML mode, which does not affect the performance of the design. Since in most cases the majority of gates in the design are not on the CPs, the increase in energy consumption of the critical paths will be negligible in comparison to the general circuit consumption. Moreover, DML static gates dissipate less power than their CMOS counterparts, resulting in reduced power dissipation of the whole design [9]. The DML key achievement is that while presenting very high performance in the dynamic mode by the proposed sizing, the same topology also enables improved energy efficiency in static mode.

2. DDFF ARCHITECTURE

Fig. 1 shows the proposed DDFF architecture. Node *X*1 is pseudo-dynamic, with a weak inverter acting as a keeper, whereas, compared to the XCFF, in the new architecture node *X*2 is purely dynamic. An unconditional shutoff mechanism is provided at the frontend instead of the conditional one in XCFF. The operation of the flip-flop can be divided into two phases: 1) the evaluation phase, when CLK is high, and 2) the precharge phase, when CLK is low [1]. The actual latching occurs during the 1–1 overlap of CLK and CLKB during the evaluation phase. If *D* is high prior to this overlap period, node *X*1 is discharged through NM0-2. This switches the state of the

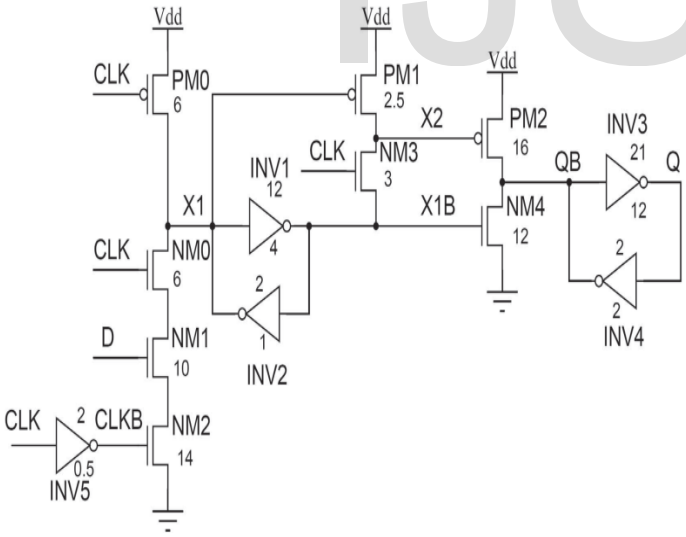

Fig.1. DDFF

cross coupled inverter pair INV1-2 causing node *X*1*B* to go high and output *QB* to discharge through *NM*4. The low level at the node *X*1 is retained by the inverter pair INV1-2 for the rest of the evaluation phase where no latching occurs. Thus, node *X*2 is held high throughout the evaluation period by the pMOS transistor *PM*1. As the CLK falls low, the circuit enters the precharge phase and node *X*1 is pulled high through *PM*0, switching the state of INV1-2. During this period node *X*2 is not actively driven by any transistor, it stores the charge dynamically. The outputs at node *QB* and maintain their voltage levels through INV3-4.

If *D* is zero prior to the overlap period, node *X*1 remains high and node *X*2 is pulled low through *NM*3 as the CLK goes high. Thus, node *QB* is charged high through *PM*2 and *NM*4 is held off. At the end of the evaluation phase, as the CLK falls low, node *X*1 remains high and *X*2 stores the charge dynamically. The architecture exhibits negative setup time since the short transparency period defined by the 1–1 overlap CLK of and CLKB allows the data to be sampled even after the rising edge of the CLK before CLKB falls low [5]. The setup time and hold time of a flip-flop refers to the minimum time period before and after the CLK edge, respectively where the data should be stable so that proper sampling is possible. Here setup time and the hold time depend on the CLK overlap period. If *VM* is the switching threshold of the inverter pair INV1-2 and *T*vm is the time required to discharge node *X*1 to *VM*, the hold time required by the flip-flop can be expressed as

$$Thold1 \geq Tvm \quad (1)$$
$$Thold0 \geq Tov - Tvm \quad (2)$$

where *T*ov is the overlap period defined by the low to high transition of the CLK and high to low transition of CLKB. It should be greater than *T*vm for the proper functioning of the flip-flop *T*hold1 and *T*hold0 represent the hold-time required for sampling a one and a zero, respectively. Also note that *T*hold1 and *T*hold0 respectively are the maximum time period after the CLK transition such that the flip-flop samples a zero and a one, respectively. Since CLKB is high prior to the low to high transition of the CLK, when *D* is high, the parasitic diffusion capacitors at the drain of *NM*1 and *NM*2 are predischarged, resulting in a low *T*vm. Now the overlap period can be chosen such that *T*hold1 and *T*hold0 in (1) and (2), respectively, are minimized.

*T*ov can be adjusted by setting proper size for the transistors in INV5 as specified in [12]. This leads to a small negative setup time and a positive hold time close to zero. Fig. 2 (a) shows hold time for sampling "zero," where *D* is held low for time-period slightly greater than *T*ov − *T*vm after the positive CLK edge. This causes node *X*1 to discharge to a voltage greater than *VM* and INV1-2 restores the high level leading to a proper latching of "zero." A similar case for sampling "one" is shown in Fig. 2 (b). Here,

since *D* is held high for a time-period equal to *T*vm, node *X*1 properly discharges and "one" is latched.

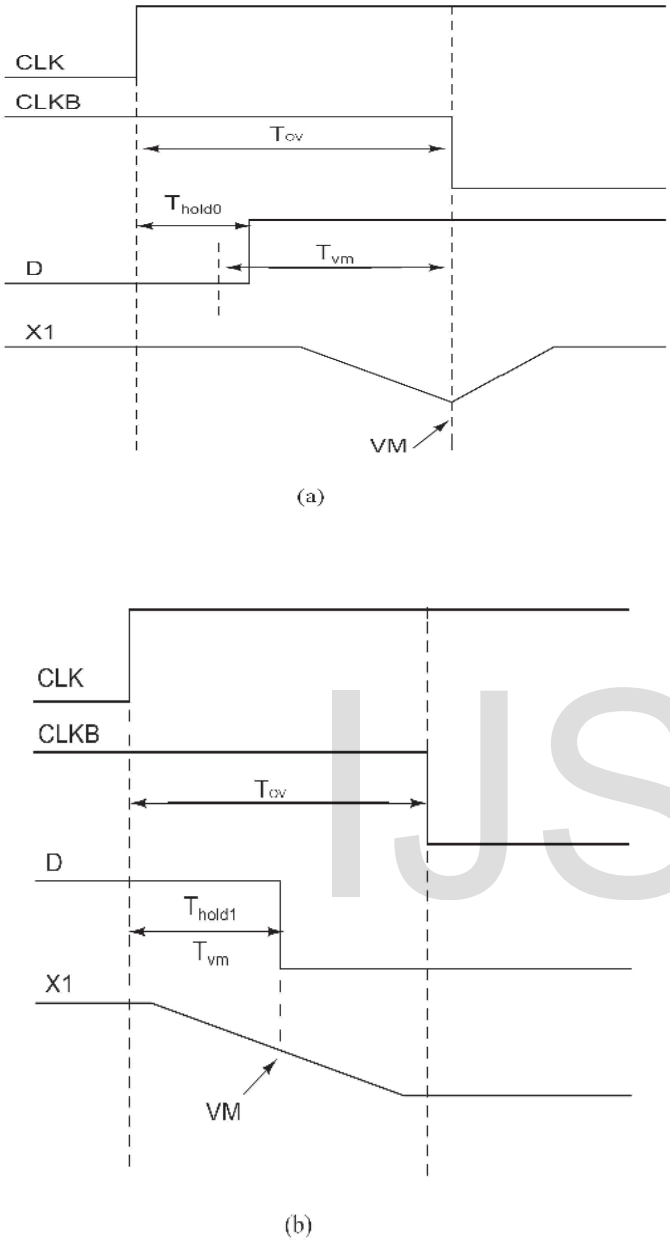

Fig. 2. Hold-time required by DDFF for sampling. (a) Zero. (b) One.

We measured *T*vm to be 18 ps in the pre-layout analysis, where only the frontend of the flip-flop was simulated with proper load, and an overlap period of 50 ps was chosen. The slight variation of the results from that of (1) and (2) is due to the nonzero slopes of CLK and data signals.

The conditional shutoff mechanism provided in SDFF is robust. It is capable of producing smaller sampling window by skewing the inverters and the NAND gate in the conditional shutoff path. Although this method can provide lower hold time requirements, it results in a larger precharge node capacitance and, hence, higher power consumption. Whereas the conditional shutoff used in XCFF causes large hold time requirement. An attempt to reduce the transparency period results in a larger size of the transistors in this path, resulting in higher capacitance on node *X*2 and hence higher power dissipation. Thus, the unconditional shutoff used in the proposed architecture provides a simple and power efficient method at the cost of a slightly involved design process. Since *T*vm plays an important role in the hold time of the proposed architecture, the worst case hold time is determined by the switching threshold of INV1-2. A larger switching threshold with a short overlap period results in a smaller *T*vm and, hence, a smaller hold time requirement.

3. DDFF-ELM

The revised structure of the proposed dual dynamic node hybrid flip-flop with logic embedding capability (DDFF-ELM) is shown in Fig.3. Note that in the revised model, the transistor driven by the data input is replaced by the PDN and the clocking scheme in the frontend is changed. The reason for this in clocking is the charge sharing, which becomes uncontrollable as the number of nMOS transistors in the stack increases. The same reason makes XCFF also incapable of embedding complex logic functions. In order to get a clear picture of the charge sharing in XCFF, it was simulated with different embedded functions and the amount of worst case charge sharing was calculated.

Fig. 3 shows the frontend pull-down structure used for incorporating a 2-input NAND and a 3-input NAND function in XCFF.

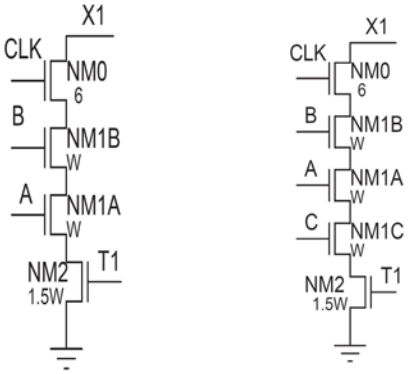

Fig. 3. 2-INPUT NAND and 3-INPUT NAND2

In a 2-input NAND embedded structure, the worst case charge sharing occurs while sampling $A = 0$, $B = 1$ following $A = B = 1$ in the previous CLK cycle. This is because all the parasitic capacitances in the pull-down path were discharged in the "11" data-sampling cycle. Similarly $A = 1$, $B = 1$, $C = 0$, causes maximum charge sharing if $A = B = C = 1$ was sampled in the previous CLK cycle, for a 3-input NAND. It can be analyzed that as the size and number of the stacked nMOS transistor increases, the charge sharing becomes uncontrollably large.

In the DDFF-ELM structure [Fig. 4], since a low to high is held high by *PM*0 making this design free from charge
sharing.

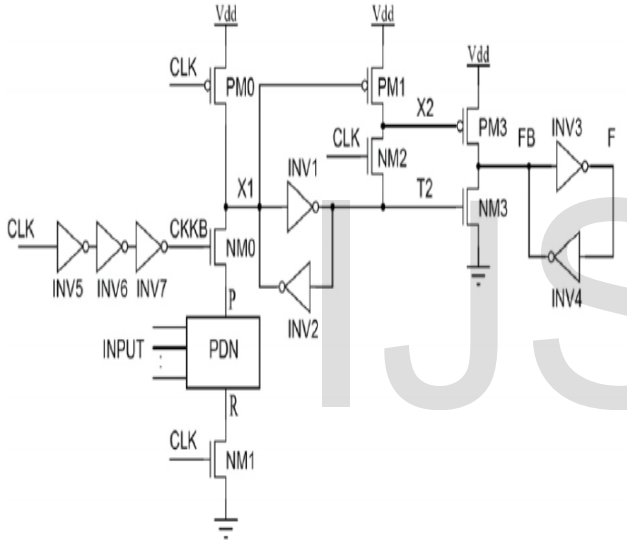

Fig.4. DDFF-ELM

The operation of the logic element is similar to the proposed DDFF. But, since CLKB is high during the precharge phase, the drain diffusion capacitances of the "on" transistors in the PDN as well as that of *NM*1 would be charged high. Thus, during the low to high transition of the CLK, comparatively larger amount of charge has to be discharged before the voltage at X1 falls below the switching threshold of INV1–2. This may require a larger overlap period, which can be obtained by using a single inverter or a cascade of three inverters depending on the complexity of the incorporated logic as shown in Fig. 4. If *T*vm is chosen for the worst case data transition in PDN, the analysis provided in (1) and (2) remains valid for the approximate estimation of the overlap period and hold-time for DDFF-ELM.

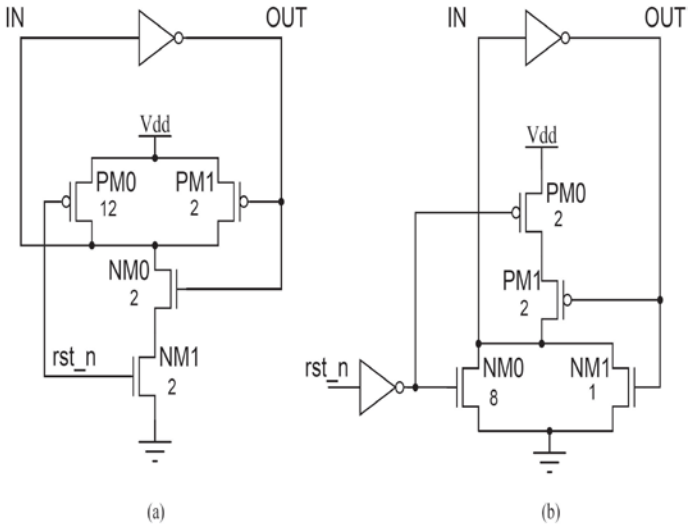

Fig.5. Incorporating asynchronous reset to logic embedded flip flops. (a) NAND-based reset circuit. (b) NOR-based reset-circuit.

As far as synchronous designs are concerned, reset functionality is inevitable. Here, we provide an area and power efficient method to incorporate asynchronous reset functionality to the DDFF-ELM. The ELM in Fig. 4 is modified to incorporate the active-low asynchronous-reset (rst_*n*) function by replacing the inverter pairs INV1-2 and INV3-4 with a NAND-based reset-circuit shown in Fig. 5(a). Nodes *I N* and OUT of two reset-circuit replaces the input and output of INV1 and INV3 of the ELM, respectively. Now, node *X*1 and *QB* are connected to *I N* and *X*1*B* and *Q* are connected to OUT of the respective reset-circuits. The NAND-based reset-circuit operates as a cross-coupled inverter-pair when rst_*n* is high. On the negative edge of rst_*n*, *PM*0 pulls node *X*1 and *QB* high and reset is achieved. Larger width is used for *PM*0 to eliminate any power consumption resulting from contention when *X*1 or *QB* is pulled low during the reset period. Also, a large *PM*0 reduces the minimum width of rst_*n* signal, required to properly reset the flip-flop. Since *PM*1, *NM*0, and *NM*1 of Fig. 5(a) are of minimum size, incorporating reset function induces a very low overhead in power and area. Although the reset function has been incorporated only for DDFF-ELM, it is applicable equally well to the DDFF. Since the comparison of ELM has to be made with that of SDFF, to

make a fair comparison, reset function has to be incorporated in SDFF.

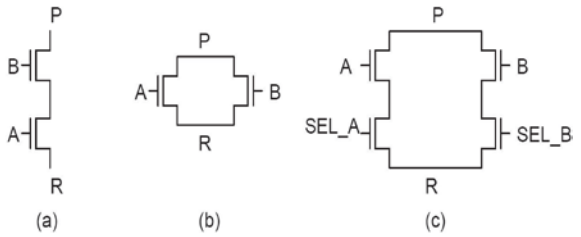

Fig.6. Embedded functions. (a) AND. (b) OR. (c) 2:1 Multiplexer.

Because of the architectural differences, the method explained earlier cannot be used for "reset" in SDFF. Thus, we use a NOR-based reset-circuit [Fig. 5(b)] in addition to NAND based reset-circuit. The function of NOR based reset-circuit is similar to that of NOR-based, except that an active high reset input is required by the former. This is achieved by inverting the rst_*n* signal as shown in Fig. 5(b). The NOR-based reset circuit acts as a cross-coupled inverter pair when rst_*n* is high, and on the negative edge of rst_*n*, *NM*0, pulls node *I N* low to achieve the required reset. For the reset of DDFF-ELM, when rst_*n* is held low for a small period of time, explains the resetting of SDFF also.

4. PERFORMANCE ANALYSIS

4.1 DDFF

To analyze the performance of DDFF, other designs were also simulated under similar conditions. Since the D-Q delay reflects the actual portion of the time period consumed by the latching device, we follow the method specified by Stojanovic and Oklobdzija [5] to consider the minimum D-Q delay as the performance metric for speed. Optimum setup-time is the data to-CLK delay when D-Q is at its minimum. As mentioned by Stojanovic and Oklobdzija [5], the power is divided into three parts–the latching power, the local CLK driving power, and the local data driving power, to accurately analyze the power performance of various designs. The simulations are carried out at various data activities to obtain a realistic performance comparison of various designs.

A data activity of 100% represents an output data transition at every positive CLK edge, and 0% represents no data transition. Since the performance of the proposed flip-flops depends on the CLK overlap period, a detailed analysis at various process and temperature corners is carried out. Since static leakage power is one of the main sources of power dissipation at scaled down technology nodes, comparison of the leakage performance of various designs has been carried out. The leakage currents for different input and output conditions are measured to find the worst case leakage power. In addition, all the designs were analyzed at different voltage points to understand the impact of supply voltage fluctuation in the functionality of the flip-flops. Finally, a 4-b synchronous up counter is designed to highlight the performance of the proposed flip-flop architecture. The reason for considering a counter is that the data activity at each bit position is known.

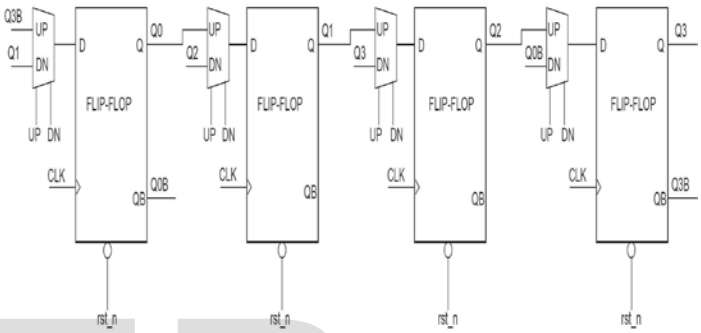

Fig.7. 4-b Johnson up-down counter.

4.2 DDFF-ELM

Various functions have been embedded into the proposed design to analyze the performance of the structure in terms of power and speed. Since SDFF is considered to be the benchmark of comparison, it was also simulated under similar conditions when embedded with the same functions. SDFF has a fast non-inverting output and a slow inverting output, whereas the proposed design has a fast inverting output and a slow non-inverting output. In order to have a fair comparison of delay, inverting and non-inverting outputs, respectively were considered for SDFF and the proposed design. AND, OR functions and a two-input multiplexer implementing the function *A.SELA + B.SELB* were embedded into both the designs by replacing the respective PDN by the structures shown in Fig. 6. Since DDFF-ELM performs the function of a flip-flop when no logic is embedded, its performance as a flip flop is compared with other flip-flops along with DDFF.

DDFF-ELM in all the above designs was designed using three inverters for generating sampling window so as to obtain the worst case timing results of the design. In order to depict the advantages of embedding logic in to the flip-flop, the combinations of static logic and flip-flop,

performing the same functions, were also designed. The performance of this discrete combination is also provided and compared with the embedded functions. In order to magnify the performance improvement of the proposed embedded logic element, a 4-b Johnson up-down counter with asynchronous reset (Fig. 7) has been designed. The counter is designed with a set of 2-input multiplexers and flip-flops. In the embedded structure, the discrete combination of multiplexer and flip-flop is replaced by a multiplexer embedded flip-flop. The ELM and the SDFF with embedded logic were incorporated with asynchronous-reset (rst_*n*) functionality.

5. DML LOGIC

In previous designs we discussed about the 4-b Johnson up-down counter used to magnify the performance improvement of DDFF-ELM. Instead of the MUX used in the counter a DML logic is proposed.

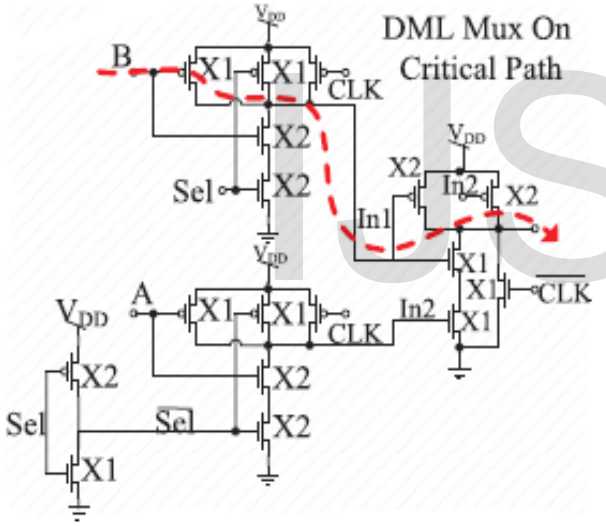

Fig.8. DML MUX on critical path

It was shown that DML gates have presented a very robust operation in both static and dynamic modes under process variations (PVT) and at low supply voltages [10], [11]. Dynamic mode robustness is mainly achieved by the intrinsic active restorer. This restorer also allows sustaining glitches, charge leakage and charge sharing. Unique sizing of the DML gate transistors is the key factor for achieving low energy consumption in the static DML mode (in which the topology of the gate is identical to the static gate). This sizing is also responsible for reduction of all capacitances of the gate. In a similar way, the unique transistor sizing enables evaluation through a low resistive network achieving fast operation in the dynamic mode. Energy efficiency is achieved in the static DML mode at the expense of slower operation (Low Energy and Low Performance, left scales). However, the dynamic mode is characterized by high performance, albeit with increased energy consumption (High Energy and High Performance, right scales). These tradeoffs allow a very high level of flexibility at the system level.

Fig. 8 shows the DML implementation of the CP. The CP flows through the first NOR (assuming that the carry in of the whole design is 0) and through all the MUXs of the design. A general DML design can be controlled (input signal driven control or external signal-driven control) to operate each gate in one of two modes: Static and Dynamic. This means that a general design can be operated in 2(*Gates Number*) different options. Switching between these two modes leads to the distinct tradeoff, meaning that the design is optimized either to achieve maximum performance or minimum energy consumption.

6. CONCLUSION

In this paper, a 4-b Johnson up-down counter with DML logic has been proposed. The DDFF and DDFF-ELM were analyzed. 4-b Johnson up-down counter was used to highlight the performance parameters of the designs and to analyze the data activity at each bit position. To improve the speed performance and to lower the power consumption, DML MUX was introduced into the counter. DML MUX operates in both static and dynamic mode. Energy efficiency can be achieved by static DML mode and higher performance can be achieved by dynamic DML mode.

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